# Millimeter Wave Receiver Comparison Under Energy vs Spectral Efficiency Trade-off

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Abstract-Receivers for mmWave systems suffer from high power consumption in Analog to Digital Converters (ADC), and there is a need to compare the three major receiver architectures: Analog, Hybrid and Digital Combining (AC, HC and DC). Moreover, the specific power consumption figure of merit of ADCs varies significantly between different component designs in the literature, so that comparisons performed for one ADC model - no matter how representative of the state of the art - do not necessarily carry over to other ADC designs with different figures of merit. In this work, we formulate a comparison method between AC, HC and DC that can be easily reproduced with different power consumption parameters and provides all information for receiver architecture selection in a compact chart figure. We also present an interpretation of the receiver selection decision problem as a multi-objective utility optimization to find the best Spectral Efficiency (SE) versus Energy Efficiency (EE) trade-off. We use existing results on the achievable rate of AC, HC and DC systems and an Additive Quantization Noise Model (AQNM) of the ADC capacity degradation. For some example commercial component parameters, we show that the usually held belief that DC requires the highest power is not valid in many cases. Rather, either DC or HC alternatively result in the better SE vs EE trade-off depending strongly on the considered component parameters and on the weight assigned to SE vs EE in the utility maximization.

Index Terms—Millimeter Wave, Analog Beamforming, Hybrid Beamforming, Digital Beamforming, Energy Efficiency, Spectral Efficiency, Low Resolution ADCs

#### I. INTRODUCTION

A 1000x increase in capacity and energy efficiency is one of the key requirements of fifth generation (5G) wireless communications. Millimeter wave (mmWave) communications, on one hand, are expected to enable greatly increased data rates in future wireless systems [1], [2]. On the other hand, although beamforming using large antenna arrays can overcome the high path-loss associated to frequencies at these wavelengths, using large antenna arrays with a wide bandwidth may lead to high power consumption, especially in the analog to digital converters (ADC) at the receiver, where energy efficiency may become a critical issue.

Power consumption of an ADC increases linearly with bandwidth and exponentially with the number of bits, and therefore may easily become the main constraint in mmWave multi-antenna receiver technologies [3]. The receiver architectures to reduce power consumption discussed so far in the literature can be categorized in three families. *Analog Combining (AC)* relies on a single Radio-Frequency (RF) chain and ADC. AC consumes the least power and is an attractive choice whenever more versatile digital processing is not really necessary [4]. *Hybrid Combining (HC)* performs combining in both the analog and the digital domains to reduce the number of RF chains and ADCs while still allowing some spatial multiplexing [5]. *Digital Combining (DC)* with low-resolution ADCs (for example, 1-4 bits) can reach a good power efficiency but at the cost of an increased quantization error [6], [7]. In this work, we study the spectral efficiency (SE) vs. energy efficiency (EE) trade-off for quantized analog, digital and hybrid receiver architectures.

The design of energy efficient multiple antenna receivers has been studied in several works. MmWave receivers with low resolution ADCs are studied in [8]–[10]. The relationship between the number of ADC bits b and the bandwidth B is studied in [11], and MIMO with low resolution is treated in [12], [13].

Comparisons among the different architectures can be found in [14], [15]. In [14], low resolution HC beamforming algorithms are designed and the energy efficiency is thoroughly studied in comparison with DC. In [15], low resolution AC, DC and HC are compared with each other and it is shown that low-resolution DC may display a better energy efficiency than HC in some scenarios.

A significant difficulty in the study of energy efficiency in large array receivers is that ADC power values are rapidly changing. A new ADC design has been recently proposed in [16] with a power consumption one order of magnitude lower than the "state of the art representative" ADCs referenced by receiver analyses such as [11], [14], [15]. Three examples of the rapid change of Walden's figure of merit (the energy consumption per conversion step per Hz) of ADCs [17] are given in Table I. In the present paper, we use the term High Power ADC (HPADC) to refer to the ADC power consumption values featured in mmWave receiver power consumption analyses such as [11]. We call Intermediate Power ADC (IPADC) the recently proposed ADC circuit [16], designed specifically for mmWave receivers. And we call Low Power ADC (LPADC) a best case scenario for ADC power consumption that can be inferred from the exhaustive survey of hardware designs in [18].

Given this extremely dynamic parameter variation, we claim that the previous literature comparing AC, HC and

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 TABLE I

 ADC WALDEN'S FIGURE OF MERIT (c) IN DIFFERENT REFERENCES

Scenario	Value	Generation
HPADC	494 fJ/step/Hz	Receiver design state of the art [11]
IPADC	65 fJ/step/Hz	Recently proposed for mmWave [16]
LPADC	5 fJ/step/Hz	Ideal future projection in survey [18]

DC in [14], [15] is incomplete in the sense that the results are only relevant as far as the "representative ADC" they selected remains the state of the art. In this work, we have focused on the design of a SE vs EE trade-off comparison chart method that is easily reproducible for different values, rather than generating results only for one chosen representative ADC model. We will give example numeric results using the values of HPADC and LPADC, and the paper is complemented by a web tool where the reader may generate a chart reproducing our analysis method using any other component parameter values [19]. Our contribution extends existing receiver analyses and comparisons in the following ways:

- First, we take into account engineers preference between SE and EE. We express this as a preference weight in a multi-objective utility maximization problem where the relative weight of SE vs EE is a free parameter. This gives new insights on the choice between HC and DC, complementing the EE comparison in [14].
- Second, we consider both Uplink and Downlink scenarios with different numbers of antennas. Our results show that in a Downlink scenario where the receiver has fewer antennas, and using the same HPADC as in [11], DC provides the best SE vs EE trade-off among all schemes. In Uplink, although HC gives the best standalone EE, DC comes quite close while allowing better SE, and thus the engineers' preference on the EE-vs-SE trade-off determines the ideal receiver.
- Third, we show that the SE vs EE trade-off is extremely parameter-dependent by comparing charts with HPADC and LPADC. This means that existing results have limited application to the specific ADC reference chosen and cannot be considered as a universal benchmark, even when the reference is very well selected.
- Fourth, we guarantee the universal reproducibility of our analysis with different component parameters by providing a web tool to complement the paper [19], where researchers can input different parameters and generate their own SE vs EE chart.

Additional results and further discussion can be found in the extended version of this paper in [20].

#### II. SYSTEM MODEL

We consider a point-to-point mmWave channel with multiple input multiple output (MIMO) antenna arrays with transmit and receive dimensions  $N_t$  and  $N_r$ , respectively. The signal has bandwidht B and a fast fading frequencyflat impulse response so that inter-symbol interference is not present. Our channel model can extend simply to frequency selective systems with multi-carrier modulations and cyclic



Figure 1. DC Receiver

prefix. We distinguish three mmWave receiver architectures with different analog or digital MIMO characteristics and ADC quantization, i.e., AC, DC and HC. For all three cases, we consider a fully digital non-quantized architecture at the transmitter. The assumption of digital transmitter is motivated by the fact that ADCs typically cause more power consumption constraints than Digital to Analog Converters. We further assume the availability of channel state information (CSI) both at the transmitter and at the receiver and we design the MIMO processing accordingly.

## A. mmWave Quantized Channel

The general received signal model is as follows:

$$\mathbf{y}_{q} = (1-\eta)(\mathbf{W}_{BB}^{H}\mathbf{W}_{RF}^{H}\mathbf{H}\mathbf{W}_{t}\mathbf{x} + \mathbf{W}_{BB}^{H}\mathbf{W}_{RF}^{H}\mathbf{n}) + \mathbf{W}_{BB}^{H}\mathbf{n}_{q}$$
(1)

where the transmitter starts with a transmitted signal x which may be scalar or in multiple dimensions and has power constraint  $E[|\mathbf{x}|^2] = P$ . The transmitter projects  $\mathbf{x}$ onto the  $N_t$  array using a unitary precoding matrix  $\mathbf{W}_t$ . The signal then passes through an  $N_t \times N_r$  random mmWave channel H with distribution defined in [21] and summarized in Table II. After propagation through the channel the receiver array captures the signal  $\mathbf{HW}_t \mathbf{x}$  and the Additive White Gaussian Noise  $\mathbf{n} \sim \mathcal{CN}(0, N_0 \mathbf{I})$ . In AC and HC, the received signal may go through an analog combining stage  $\mathbf{W}_{RF}$  where only phase-shifting and addition are permitted (each coefficient of the matrix is a phase change  $\{\mathbf{W}_{RF}\}_{i,j} = e^{j\theta_{i,j}} \forall i \in \{1..., N_t\} \forall j \in \{1..., N_r\}$ ). The analog signal in each RF chain is converted at the ADCs and finally goes through digital combining  $\mathbf{W}_{BB}$ . We model the quantization distortion of the signal using the additive quantization noise model (AQNM) [22], in which a noise term  $\mathbf{n}_q$  is added before digital combining. We denote by  $\eta$ the inverse of the signal-to-quantization noise ratio, which is inversely proportional to the square of the resolution of an ADC. For a Gaussian input distribution, the values of  $\eta$  for  $b \leq 5$  (where b is the number of ADC bits) are listed in Table III, and for b > 5 can be approximated by  $\eta = \frac{\pi\sqrt{3}}{2} 2^{-2b}$  [12].

## B. Digital Combining (DC) Receiver

The fully digital receiver is shown in Figure 1. DC has a dedicated RF chain per antenna element, and in the channel model (1) we have that  $\mathbf{W}_t$  and  $\mathbf{W}_{BB}$  are  $N_t \times N_t$  digital precoding and  $N_r \times N_r$  digital combining matrices, whereas analog processing is absent so that  $\mathbf{W}_{BF} = \mathbf{I}_{N_r}$ .

We compute the DC matrices using the singular value decomposition of the channel matrix  $\mathbf{H} = \mathbf{U}\Sigma\mathbf{V}^{H}$ . By

TABLE II MMWAVE CHANNEL PROBABILITY DISTRIBUTION [21]

$$\mathbf{H} = \sqrt{\frac{N_t N_r}{\rho N_c N_p}} \sum_{k=1}^{N_c} \sum_{\ell=1}^{N_p} g_{k,\ell} \mathbf{a}_r(\phi_k + \Delta \phi_{k,\ell}) \mathbf{a}_t^H(\theta_k + \Delta \theta_{k,\ell})$$



applying precoding  $\mathbf{W}_t = \mathbf{V}$  and combining  $\mathbf{W}_{BB} = \mathbf{U}^H$ , we create an equivalent diagonal channel where the transmit power P may be allocated across the singular values  $\Sigma$ . With this formulation, the rate maximization problem with DC is given as

$$C_{DC} = \mathbf{E}_{\mathbf{H}} \left[ \max_{\mathbf{R}_{\mathbf{x}\mathbf{x}}} B \log_2 \det \left| \mathbf{I} + (1 - \eta) \Sigma \mathbf{R}_{\mathbf{x}\mathbf{x}} \Sigma^H \right| \\ (N_o \mathbf{I} + \eta \mathbf{U}^H \operatorname{diag}(\mathbf{U} \Sigma \mathbf{R}_{\mathbf{x}\mathbf{x}} \Sigma^H \mathbf{U}^H) \mathbf{U})^{-1} \right|$$
(2)

where the input covariance matrix  $\mathbf{R}_{\mathbf{x}\mathbf{x}}$  that maximizes the rate is obtained using the water-filling algorithm.

The power consumption of the DC architecture is

$$P_{Tot}^{DC} = N_r (P_{LNA} + P_{RF} + 2P_{ADC}) \tag{3}$$

where  $P_{RF} = P_M + P_{LO} + P_{LPF} + P_{BB_{amp}}$ .

In this paper we use an example of component power consumptions detailed in Table IV, but other values may also be applied depending on the advances in hardware design.  $P_{ADC}$  increases exponentially with *b* and linearly with *B* and with the ADC Walden's figure of merit *c* [23]. The power consumption of all the other components is independent of the bandwidth and the number of bits.

Finally, we define the EE of each receiver as  $EE \triangleq \frac{C}{P_{Tot}}$ , where C is the achievable rate and  $P_{Tot}$  represents the total power consumption.

## C. Analog Combining (AC) Receiver

The fully analog receiver is shown in Figure 2. In contrast to a DC, all receiver processing is performed in the analog domain and only one RF chain and ADC pair are needed. We have that in (1),  $\mathbf{W}_t$  and  $\mathbf{W}_{RF}$  are  $1 \times N_t$  digital precoding and  $N_r \times 1$  analog combining matrices, and digital combining is absent ( $\mathbf{W}_{BB} = 1$ ).

TABLE IV Power consumption of each device

Device	Notation	Value
Low Noise Amplifier (LNA) [24]	$P_{LNA}$	39 mW
Splitter and Combiner [24]	$P_{SP}$ and $P_C$	19.5 mW each
Phase shifter [25], [26]	$P_{PS}$	2 mW or 0
Mixer [27]	$P_M$	16.8 mW
Local oscillator [28]	$P_{LO}$	5  mW
Low pass filter [28]	$P_{LPF}$	14 mW
Base-band amplifier [28]	$P_{BB_{amn}}$	5  mW
ADC [23]	$P_{ADC}$	$cB2^b$



Figure 2. AC Receiver

The rate maximization problem with AC is given as

$$C_{AC} = \mathbf{E}_{\mathbf{H}} \left[ \max_{\mathbf{w}_{r}, \mathbf{w}_{t}} B \log_{2} \left( 1 + \frac{(1-\eta) |\mathbf{w}_{r}^{H} \mathbf{H} \mathbf{w}_{t}|^{2} P}{N_{o} + \eta |\mathbf{w}_{r}^{H} \mathbf{H} \mathbf{w}_{t}|^{2} P} \right) \right]$$
  
s.t.  $|w_{r,i}| = \frac{1}{\sqrt{N_{r}}}, ||\mathbf{w}_{t}||^{2} = 1,$  (4)

Here we may first work out the digital precoding, which only has a unitary power constraint. We choose  $\mathbf{w}_t$  to maximize the gain under any given value of  $\mathbf{w}_r$  using  $\mathbf{w}_t = \frac{\mathbf{H}^H \mathbf{w}_r}{||\mathbf{H}^H \mathbf{w}_r||^2}$ . Secondly, in unconstrained circumstances the optimal  $\mathbf{w}_r$  would be the maximum left eigenvector  $(\mathbf{u}_{max})$ of  $\mathbf{H}$ , however, due to the constant amplitude constraint  $\mathbf{w}_r$ can only be a phase projection of it, i.e.

$$\tilde{\mathbf{w}}_{r}^{H} = \frac{1}{\sqrt{N_{r}}} (e^{\measuredangle u_{\max}^{1}}, e^{\measuredangle u_{\max}^{2}}, \dots e^{\measuredangle u_{\max}^{N_{r}}})^{T}$$
(5)

The power consumption of AC is evaluated as

$$P_{Tot}^{AC} = N_r (P_{LNA} + P_{PS}) + P_{RF} + P_C + 2P_{ADC} \quad (6)$$

#### D. Hybrid Combining (HC) Receiver

The hybrid receiver is shown in Figure 3. We have that in (1),  $\mathbf{W}_t$ ,  $\mathbf{W}_{RF}$  and  $\mathbf{W}_{BB}$  are  $N_{RF} \times N_t$  digital precoding,  $N_r \times N_{RF}$  analog combining and  $N_{RF} \times N_{RF}$  digital combining matrices, respectively. The analog combining is obtained using Algorithm 1 from [29], and the digital precoding and combining use the Singular Value Decomposition as in the DC model, over an equivalent channel  $\mathbf{W}_{RF}\mathbf{H}$  with dimensions  $N_t \times N_{RF}$ 

The achievable rate maximization with HC is given as

$$C_{HC} = \mathbf{E}_{\mathbf{H}} \left[ \max_{\mathbf{R}_{\mathbf{x}\mathbf{x}}} B \log_2 \det \left| \mathbf{I} + (1 - \eta) \Sigma \mathbf{R}_{\mathbf{x}\mathbf{x}} \Sigma^H \right| \\ (N_o \mathbf{I} + \eta \mathbf{U}^H \operatorname{diag}(\mathbf{U} \Sigma \mathbf{R}_{\mathbf{x}\mathbf{x}} \Sigma^H \mathbf{U}^H) \mathbf{U})^{-1} \right|$$
(7)



Figure 3. HC Receiver

## Algorithm 1 Alternate projection $W_{RF}$ design

Initialize  $\mathbf{W}_{SU} = [\mathbf{u}_1 \dots \mathbf{u}_{N_{RF}}] \in \mathbf{U}$ , where  $\mathbf{H} = \mathbf{U} \Sigma \mathbf{V}^H$ while not converging **do**  $[\tilde{\mathbf{W}}_{RF}]_{ij} = \frac{1}{\sqrt{N_r}} \exp(j \measuredangle [\mathbf{W}_{SU}]_{ij}), \forall i, j$  $\mathbf{W}_{SU} = (\tilde{\mathbf{W}}_{RF} \tilde{\mathbf{W}}_{RF}^*)^{-\frac{1}{2}} \tilde{\mathbf{W}}_{RF}$ end while

Note that  $C_{HC}$  is upper bounded by  $C_{DC}$  due to the fact that  $\mathbf{W}_{RF}$  has analog constraints and  $N_{RF} \leq N_r$ .

Finally, the power consumption of HC is evaluated as

$$P_{Tot}^{HC} = N_r (P_{LNA} + P_{SP} + N_{RF} P_{PS}) + N_{RF} (P_{RF} + P_C + 2P_{ADC})$$
(8)

## III. SE VS EE ANALYSIS AND EXAMPLES

We plot the EE vs SE curves for each receiver as b increases from 1 to 8 at increments of 1. The top of the chart corresponds to highest SE and the rightmost points correspond to highest EE. Thus, an ideal goal would be to design a receiver that is as close to the top right corner of the chart as possible. Nonetheless, this intuitive guideline is not sufficient to capture the needs of receiver design when a trade-off between EE and SE exists. We construct a multi-objective utility optimization interpretation of the receiver selection problem that serves to discuss the interpretation of the chart. Note that this optimization is easy to solve due to the small search space, and its value is not in the result itself but in the interpretation it gives to the chart.

We consider a free parameter  $\alpha \in [0, 1]$  that represents the receiver designer's preference between higher EE and higher SE. The "receiver utility" according to the designer's preference can be expressed and maximized as

$$U = \max_{\{HC, DC, AC\}} \max_{b \in \{1...8\}} \alpha \text{EE} + (1 - \alpha) \text{SE} \qquad (9)$$

where  $\alpha = 0$  is SE maximization and  $\alpha = 1$  is EE maximization. Since the problem is relatively easy, we can obtain the set of solutions for the entire range of parameters  $\alpha \in [0, 1]$ , where the solutions in the set correspond to all the receiver designs that are valuable for some kind of receiver designer preference. Receivers not in the set of solutions for all  $\alpha \in [0, 1]$  are receivers that would never be preferred by any designer.

We obtain SE vs EE charts for AC, HC and DC receivers with b ranging from 1 to 8 in four scenarios, i.e., combining Downlink and Uplink with low and high SNR. We highlight the points that are utility maximization solutions in the SE-vs-EE charts to distinguish the most valuable receiver designs from the rest. For Uplink, we use  $N_t = 16$  and  $N_r = 64$ , and for Downlink, we use  $N_t = 64$  and  $N_r = 16$ . For high SNR we consider 0 dB before combining, which is about 100 m distance in LOS mmWave pathloss, and for low SNR we consider -20 dB which is about the same distance with NLOS. We have also introduced different numbers of RF chains in HC to observe the impact of a good selection of the dimension of the hybrid system. Increasing  $N_{RF}$  increases SE but also the power consumption, potentially leading to a drop in EE.

We give two examples with two different sets of component parameters<sup>1</sup>:

- The High Power ADC (HPADC) model is based on an existing device that supports sampling at Gs/s and has been referenced in related literature such as [11]. In order to give HC Phase Shifters appropriate power consumption values, we pair the HPADC model with an existing PS model, i.e., with  $P_{PS} = 2$ mW, referenced in [25]. In this example we focus on comparing the different receivers and on the impact of Downlink/Uplink in high/low SNR scenarios. The results validate the observations from [11], [14] and also provide some additional insights about HPADC.
- The Low Power ADC (LPADC) model considers a likely best-case scenario deduced from the hardware survey in [18]. Likewise, we pair this best-case scenario for ADCs with a best case phase shifter model, with negligible power consumption ~ 0 mW, as in [26]. For the second example, we focus on displaying how critically parameter-dependent the receiver EE-vs-SE trade-off comparison is. We show how the observations from the same example change drastically and the results in [11], [14] for HPADC cannot be generalized to different ADC components in the literature.

Additional results and more examples and discussion can be found in the extended version of this paper [20].

#### A. Example 1: High power ADC characteristics

We plot the SE vs EE for the three receiver architectures with HPADC in Fig. 4. Since ADCs have high power consumption, as b is increased the lines first reach upward and right, and then steer left and EE returns to the left corner while SE continues rising. This is consistent with results in [14], [20] that show that SE is monotonic in b whereas EE reaches a maximum and then drops. Note that the points maximizing (9) for different values of  $\alpha \in [0, 1]$ are highlighted, so the set of highlighted points in the chart can be regarded as a collection of "all the interesting receivers".

Note that the number of bits that maximizes SE is not necessarily the same that maximizes EE. For instance, for DC in Figure 4(a) the point in the top left corner corresponds to b = 8 and maximizes SE (it is highlighted for  $\alpha =$ 

<sup>&</sup>lt;sup>1</sup>Although we did not fabricate the receivers (i.e., AC, DC or HC) in hardware, the power consumption model we employ is based on hardware designs considered in recent papers, e.g., [11], [15].



Figure 4. SE vs. EE comparison for AC, DC and HC schemes with a HPADC model and with  $N_{RF} = 2, 4, 8, 10, 12$  for HC. In the Downlink,  $\max(N_{RF})$  is set to 10 as a further increase would only decrease the EE of HC without any significant SE improvement.

0), whereas the rightmost point corresponding to b = 5 maximizes EE (it is highlighted for  $\alpha = 1$ ). Notice also that the number of bits that maximizes either magnitude varies for different receivers. For example AC, HC with  $N_{RF} = 4$ , and DC achieve maximum EE with b = 7, 6 and 5, respectively.

In Fig. 4(a) for high SNR Downlink we have a result in which DC completely outperforms all other schemes. DC with 4 or 5 bits has the best EE, and with 8 bits has the best SE. Note that only DC points are selected across all values of  $\alpha \in [0, 1]$ , always achieving the best EE vs SE trade-off. The higher number of antennas in Uplink causes an increase in power consumption that affects DC more severely. In Fig. 4(b) the high SNR Uplink HC using  $N_{RF} = 8$  with 6-8 bits achieves greater or equal EE than the best EE of DC. However, HC is only selected with 6-7 bits for the lowest values of  $\alpha$ , whereas DC not only is chosen for maximum SE (b = 8), but also offers the best trade-off with good SE and good EE for mid-range values of  $\alpha$  (b = 5, 6).

To observe the impact of SNR in Downlink we compare Figures 4(a) and 4(c). At high SNR spatial multiplexing offers significant rate gains, and HC SE rises significantly as  $N_{RF}$  grows from 2 to 10 while EE does not contract very much. The HC scheme with the best EE uses  $N_{RF} = 4$ and b = 6, yet DC still manages to completely outperform HC with any number of RF chains. At low SNR, however, there is no significant spatial multiplexing advantage, and HC SE grows when  $N_{RF}$  steps from 2 to 4, but becomes flat thereafter, while EE keeps retracting. Nonetheless, it is at low SNR where we observe a non-DC scheme to get a point in the optimal set for the first time. This scheme is AC which is very well suited for low-SNR scenarios because it pools all the transmitter energy into the strongest propagation direction and has very low component power consumption. Notice that for HC schemes the optimal number of RF chains is SNR-dependent, which is an additional handicap for the use of HC designs, since usually the same hardware design is used in all the devices at different distances in a network. The only Downlink scenario where HC achieves an EE similar to DC is with  $N_{RF} = 2$  and b = 2, and yet its SE is 6% lower.

The HC receiver works much better in Uplink, as we can see comparing Figures 4(b) and 4(d). Here we observe again that as  $N_{RF}$  takes values 2, 4, 8 and 12 the SE of HC grows at high SNR and becomes flat at low SNR. At high SNR,  $N_{RF} = 8$  HC achieves the best EE and  $N_{RF} = 12$  contributes a point with good EE-vs-SE trade-off, while DC provides other good points in the trade-off and result in the highest SE. However at low SNR  $N_{RF} = 4$  is the only HC configuration that outperforms DC in a trade-off point,



Figure 5. SE vs. EE comparison for AC, DC and HC schemes with a LPADC model and with  $N_{RF} = 2, 4, 8, 10, 12$  for HC.

and the best EE is again provided by AC. As in Downlink, note that the SNR dependence of the optimal  $N_{RF}$  can be an issue for HC, and a wrong choice of  $N_{RF}$  by a small difference makes the HC receiver worse than DC.

Finally, if we wish to add a constant device power consumption ruler we can superimpose it with diagonal dotted lines. In Downlink, only AC is viable under 1 W, whereas above 1 W DC outperforms the other schemes. In Uplink, only AC is viable under 3 W, HC presents a better choice in the range 3-8 W and DC outperforms all schemes above 8 W. Surprisingly, DC is a better receiver for both smaller devices (UE with 1-3 W) and large devices (macro cell BS with 10-50 W), while HC is better for mid-range power devices (such as a pico cell BS with 3-10W). In devices below 1 W AC seems to be the only viable option.

#### B. Example 2: Low power ADC characteristics

Note that all the observations made about Figure 4 apply only to receivers fabricated with the component parameters in Table IV and the HPADC in Table I. A significant contribution of our analysis chart is its versatility to reproduce the analysis with changed parameters. In Figure 5 we represent the same analysis performed with the LPADC model and 0 W power consumption for phase shifters, as a sort of "future expected values". Since ADCs have lower power consumption, as b is increased the lines progress to the top right and, differently from HPADC, EE always increases with b in LPADC. Also, now the number of bits that maximizes SE for a receiver also maximizes EE.

In Fig. 5(a) for high SNR Downlink we have a result in which DC completely outperforms all schemes and there is no trade-off. DC with 8 bits is significantly above in terms of both EE and SE. For the Uplink in Fig. 5(b) there is a slight trade-off in which points are very close. HC with  $N_{RF} = 8$  achieves slightly better EE with slightly worse SE, and DC with b = 7 is chosen for some value of  $\alpha$ .

To observe the impact of SNR in Downlink we compare Figures 5(a) and 5(c). We observe again the saturation of HC SE as  $N_{RF}$  grows from 2 to 10 at low SNR although it grows at high SNR. Moreover, DC remains the dominant receiver in most trade-off preferences except if one sets  $\alpha =$ 1, where AC is chosen with a tiny gain in EE and a huge 50% drop in SE. Cases such as AC here exemplify why a trade-off utility maximization interpretation can lead to new insights on the receiver selection problem.

Looking at the Uplink we compare the high and low SNR cases in Figures 5(b) and 5(d), respectively. Here we observe again the saturation of HC with an increase of  $N_{RF}$  in low SNR and the issue that the optimal  $N_{RF}$  is SNR-dependent. In addition, mismatched  $N_{RF}$ 's are outperformed by DC. Furthermore, AC offers slightly better EE with a huge SE drop, HC contributes a couple of points in the trade-off, and DC contributes most of the points in the EE-vs-SE trade-off.

Finally, with regard to power consumption, the same observations we made for HPADC apply here.

## **IV. CONCLUSIONS**

In this work, we studied and compared the spectral and energy efficiencies of Analog, Digital and Hybrid combining schemes. We considered receivers operating at mmWave and equipped with low resolution analog to digital converters (ADC). We developed a multi-objective optimization formulation, where the preference between SE and EE is weighted by a free parameter. This allows researchers/designers to identify the best receiver scheme depending on their needs.

We considered both Uplink and Downlink scenarios, and our results showed that in the Downlink, where the receiver is equipped with fewer antennas, DC outperforms other schemes, whereas in the Uplink there is a trade-off between HC and DC. Moreover, in low SNR scenarios AC achieves the highest EE, at the expense of severe drops in SE.

We also argued that the EE vs SE comparison among different receiver designs is extremely parameter dependent, and results based on one chosen set of parameter values do not represent a complete picture due to the fact that ADCs and other component circuits are rapidly improving. To illustrate this, we produced comparison charts with low power and high power ADCs and showed that the SE vs EE trade-off results differ significantly. Therefore, ADCs and other component parameters directly affect the choice of the most appropriate combining scheme. To address the effect of this critical parameter dependency, we developed an easily reproduced analysis method in chart form and provided a web tool to complement this paper, where the readers may obtain their own SE vs EE trade-off charts by plugging in the set of parameter values for the hardware components they have available.

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